C106 Series

Preferred Device

Sensitive Gate Silicon Controlled Rectifiers

Reverse Blocking Thyristors

Glassivated PNPN devices designed for high volume consumer applications such as temperature, light, and speed control; process and remote control, and warning systems where reliability of operation is important.

- Glassivated Surface for Reliability and Uniformity
- Power Rated at Economical Prices
- Practical Level Triggering and Holding Characteristics
- Flat, Rugged, Thermopad Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Sensitive Gate Triggering
- Device Marking: Device Type, e.g., C106B, Date Code

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off–State Voltage(1) (Sine Wave, 50–60 Hz, R_{GK} = 1 kΩ, T_C = –40° to 110°C) C106B C106D, C106D1 C106M, C106M1	V_{DRM}, V_{RRM}	200 400 600	Volts
On-State RMS Current (180° Conduction Angles, T_C = 80°C)	$I_{T(RMS)}$	4.0	Amps
Average On–State Current (180° Conduction Angles, T_C = 80°C)	$I_{T(AV)}$	2.55	Amps
Peak Non-Repetitive Surge Current (1/2 Cycle, Sine Wave, 60 Hz, T_J = +110°C)	I_{TSM}	20	Amps
Circuit Fusing Considerations (t = 8.3 ms)	I^2t	1.65	A^2s
Forward Peak Gate Power (Pulse Width ≤ 1.0 μsec, T_C = 80°C)	P_{GM}	0.5	Watt
Forward Average Gate Power (Pulse Width ≤ 1.0 μsec, T_C = 80°C)	$P_{G(AV)}$	0.1	Watt
Forward Peak Gate Current (Pulse Width ≤ 1.0 μsec, T_C = 80°C)	I_{GM}	0.2	Amp
Operating Junction Temperature Range	T_J	–40 to +110	°C
Storage Temperature Range	T_{stg}	–40 to +150	°C
Mounting Torque(2)	—	6.0	in. lb.

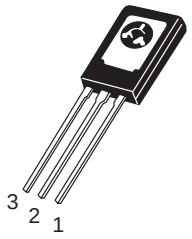
(1) V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; however, positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

(2) Torque rating applies with use of compression washer (B52200F006). Mounting torque in excess of 6 in. lb. does not appreciably lower case-to-sink thermal resistance. Anode lead and heatsink contact pad are common.

ON Semiconductor

http://onsemi.com

SCRs
4 AMPERES RMS
200 thru 600 VOLTS



TO–225AA
(formerly TO–126)
CASE 077
STYLE 2

PIN ASSIGNMENT	
1	Cathode
2	Anode
3	Gate

ORDERING INFORMATION

Device	Package	Shipping
C106B	TO225AA	500/Box
C106D	TO225AA	500/Box
C106D1	TO225AA	500/Box
C106M	TO225AA	500/Box
C106M1	TO225AA	500/Box

Preferred devices are recommended choices for future use and best overall value.

THERMAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.0	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	°C/W
Maximum Lead Temperature for Soldering Purposes 1/8″ from Case for 10 Seconds	T_L	260	°C

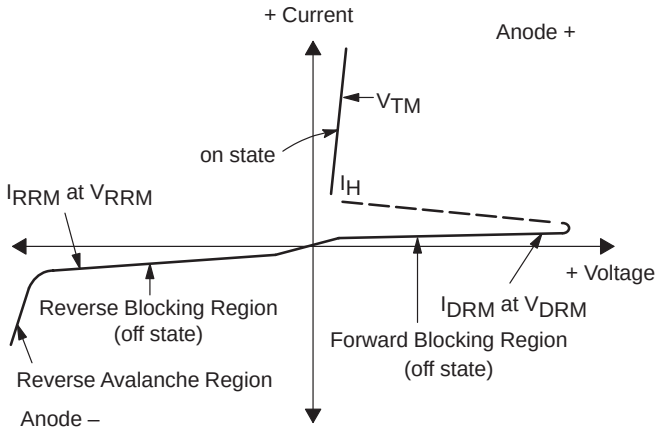
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Peak Repetitive Forward or Reverse Blocking Current (V_{AK} = Rated V_{DRM} or V_{RRM}, R_{GK} = 1000 Ohms)	T_J = 25°C T_J = 110°C	I_{DRM}, I_{RRM}	— —	— —	10 100	μA μA
ON CHARACTERISTICS						
Peak Forward On–State Voltage(1) (I_{FM} = 1 A Peak for C106B, D, & M) (I_{FM} = 4 A Peak for C106D1, & M1)		V_{TM}	—	—	2.2	Volts
Gate Trigger Current (Continuous dc)(2) (V_{AK} = 6 Vdc, R_L = 100 Ohms)	T_J = 25°C T_J = –40°C	I_{GT}	— —	15 35	200 500	μA
Peak Reverse Gate Voltage (I_{GR} = 10 μA)		V_{GRM}	—	—	6.0	Volts
Gate Trigger Voltage (Continuous dc)(2) (V_{AK} = 6 Vdc, R_L = 100 Ohms)	T_J = 25°C T_J = –40°C	V_{GT}	0.4 0.5	.60 .75	0.8 1.0	Volts
Gate Non–Trigger Voltage (Continuous dc)(2) (V_{AK} = 12 V, R_L = 100 Ohms, T_J = 110°C)		V_{GD}	0.2	—	—	Volts
Latching Current (V_{AK} = 12 V, I_G = 20 mA)	T_J = 25°C T_J = –40°C	I_L	— —	.20 .35	5.0 7.0	mA
Holding Current (V_D = 12 Vdc) (Initiating Current = 20 mA, Gate Open)	T_J = 25°C T_J = –40°C T_J = +110°C	I_H	— — —	.19 .33 .07	3.0 6.0 2.0	mA
DYNAMIC CHARACTERISTICS						
Critical Rate–of–Rise of Off–State Voltage (V_{AK} = Rated V_{DRM}, Exponential Waveform, R_{GK} = 1000 Ohms, T_J = 110°C)		dv/dt	—	8.0	—	V/μs

(1) Pulse Test: Pulse Width ≤ 2.0 ms, Duty Cycle ≤ 2%.
(2) R_{GK} is not included in measurement.

Voltage Current Characteristic of SCR

Symbol	Parameter
V_{DRM}	Peak Repetitive Off State Forward Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Off State Reverse Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Peak On State Voltage
I_H	Holding Current



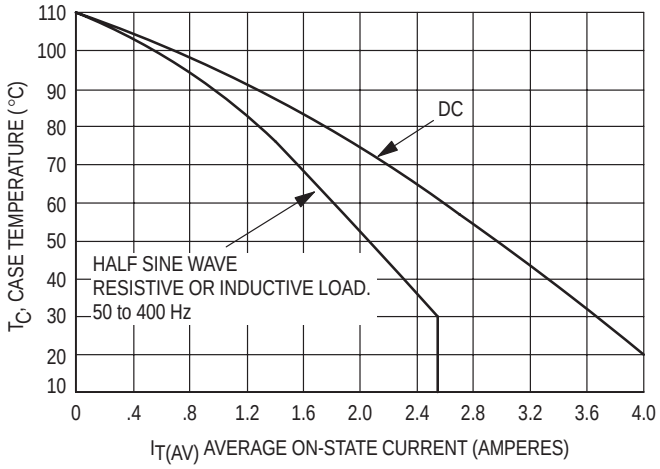


Figure 1. Average Current Derating

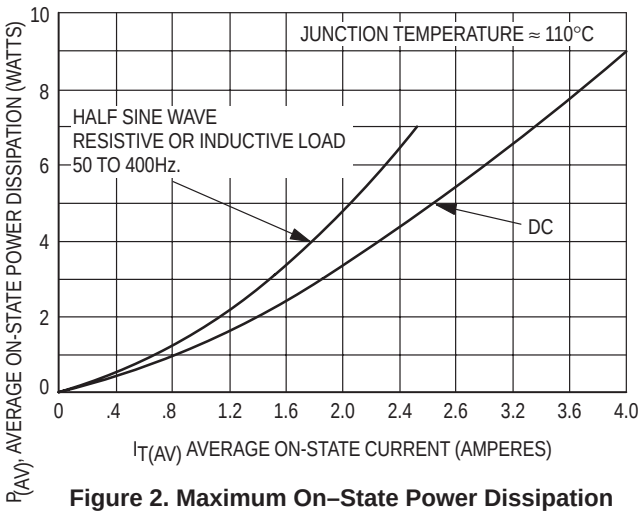


Figure 2. Maximum On–State Power Dissipation

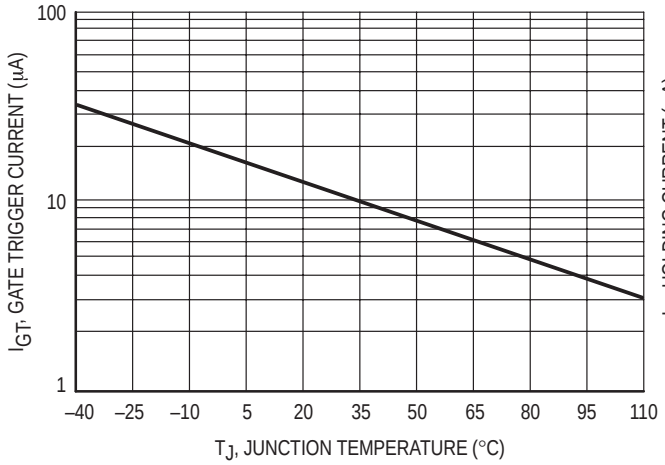


Figure 3. Typical Gate Trigger Current versus Junction Temperature

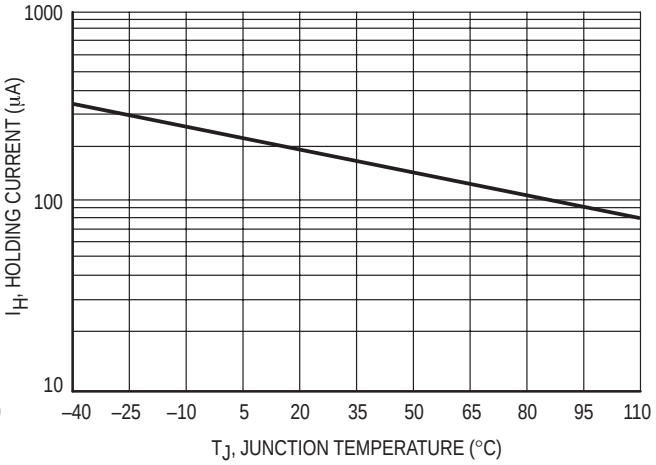


Figure 4. Typical Holding Current versus Junction Temperature

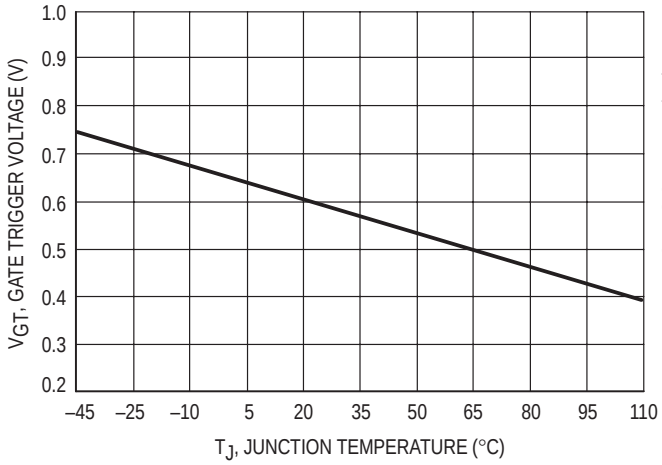


Figure 5. Typical Gate Trigger Voltage versus Junction Temperature

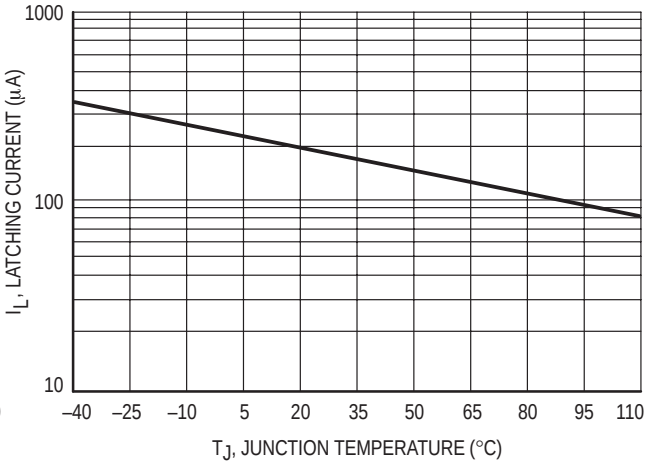
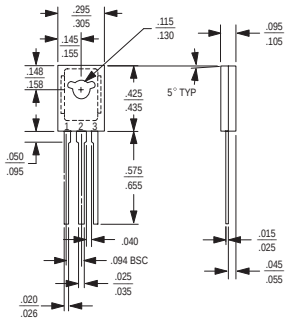


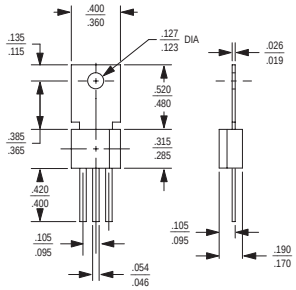
Figure 6. Typical Latching Current versus Junction Temperature

Package Interchangeability

The dimensional diagrams below compare the critical dimensions of the ON Semiconductor C-106 package with competitive devices. It has been demonstrated that the smaller dimensions of the ON Semiconductor package make it compatible in most lead-mount and chassis-mount applications. The user is advised to compare all critical dimensions for mounting compatibility.



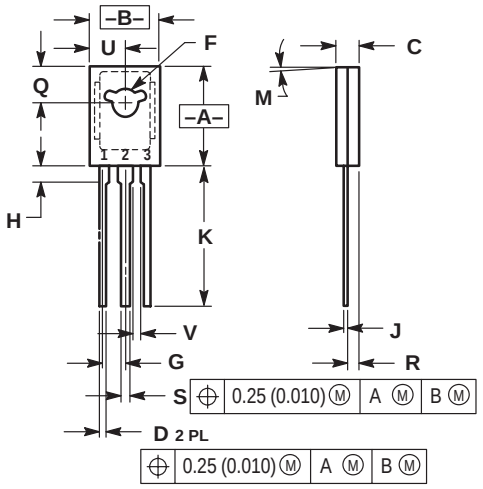
ON Semiconductor C-106 Package



Competitive C-106 Package

PACKAGE DIMENSIONS

TO–225AA
(formerly TO–126)
CASE 077–09
ISSUE W



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.425	0.435	10.80	11.04
B	0.295	0.305	7.50	7.74
C	0.095	0.105	2.42	2.66
D	0.020	0.026	0.51	0.66
F	0.115	0.130	2.93	3.30
G	0.094 BSC		2.39 BSC	
H	0.050	0.095	1.27	2.41
J	0.015	0.025	0.39	0.63
K	0.575	0.655	14.61	16.63
M	5° TYP		5° TYP	
Q	0.148	0.158	3.76	4.01
R	0.045	0.065	1.15	1.65
S	0.025	0.035	0.64	0.88
U	0.145	0.155	3.69	3.93
V	0.040	—	1.02	—

STYLE 2:
PIN 1. CATHODE
2. ANODE
3. GATE

Notes

PUBLICATION ORDERING INFORMATION

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