- **High Degree of Linearity**
- **High On-Off Output Voltage Ratio**
- **Low Crosstalk Between Switches**
- **Low On-State Impedance . . . 50-Ω TYP at V_{CC} = 6 V**
- **Individual Switch Controls**
- **Extremely Low Input Current**

**D, DB, N, OR PW PACKAGE
(TOP VIEW)**

```
        ┌───┬─┐
  1A ──┤1    14├── V_CC
  1B ──┤2    13├── 1C
  2B ──┤3    12├── 4C
  2A ──┤4    11├── 4A
  2C ──┤5    10├── 4B
  3C ──┤6     9├── 3B
 GND ──┤7     8├── 3A
        └─────┘
```
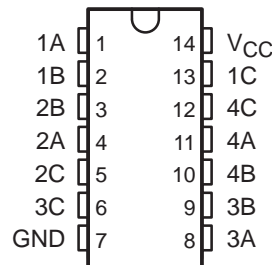
description

The SN74HC4066 is a silicon-gate CMOS quadruple analog switch designed to handle both analog and digital signals. Each switch permits signals with amplitudes of up to 6 V (peak) to be transmitted in either direction.

Each switch section has its own enable input control (C). A high-level voltage applied to C turns on the associated switch section.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	PDIP – N	Tube	SN74HC4066N	SN74HC4066N
	SOIC – D	Tube	SN74HC4066D	HC4066
		Tape and reel	SN74HC4066DR	
	SSOP – DB	Tape and reel	SN74HC4066DBR	HC4066
	TSSOP – PW	Tape and reel	SN74HC4066PWR	HC4066

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each switch)

INPUT CONTROL (C)	SWITCH
L	OFF
H	ON

Copyright © 2000, Texas Instruments Incorporated

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

1
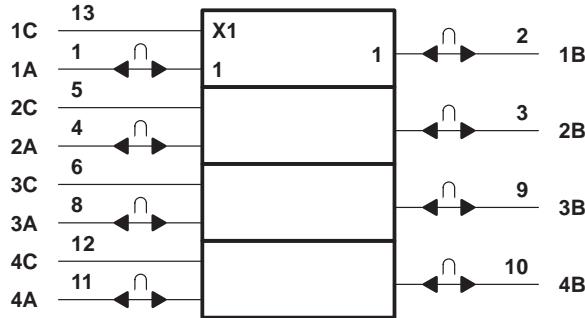
logic symbol[†]

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each switch (positive logic)

One of Four Switches
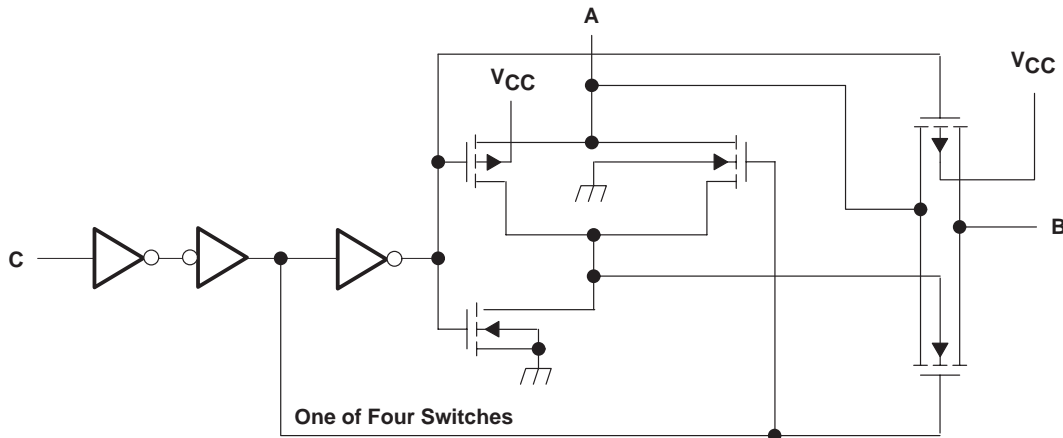
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[‡]

Supply voltage range, V_{CC} (see Note 1) . . . . −0.5 V to 7 V
Control-input diode current, I_I (V_I < 0 or V_I > V_{CC}) . . . . ±20 mA
I/O port diode current, I_I (V_I < 0 or $V_{I/O}$ > V_{CC}) . . . . ±20 mA
On-state switch current ($V_{I/O}$ = 0 to V_{CC}) . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package . . . . 86°C/W
                                                     DB package . . . . 96°C/W
                                                     N package . . . . 80°C/W
                                                     PW package . . . . 113°C/W
Storage temperature range, T_{stg} . . . . −65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
   functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
   implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. All voltages are with respect to ground unless otherwise specified.
        2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		$2^\dagger$	5	6	V
$V_{I/O}$	I/O port voltage		0		V_{CC}	V
V_{IH}	High-level input voltage, control inputs	V_{CC} = 2 V	1.5		V_{CC}	V
		V_{CC} = 4.5 V	3.15		V_{CC}	
		V_{CC} = 6 V	4.2		V_{CC}	
V_{IL}	Low-level input voltage, control inputs	V_{CC} = 2 V	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	
		V_{CC} = 6 V	0		1.2	
t_t	Input rise/fall time	V_{CC} = 2 V			1000	ns
		V_{CC} = 4.5 V			500	
		V_{CC} = 6 V			400	
T_A	Operating free-air temperature		−40		85	°C

† With supply voltages at or near 2 V, the analog switch on-state resistance becomes very nonlinear. It is recommended that only digital signals be transmitted at these low supply voltages.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
R_{on}	On-state switch resistance	I_T = −1 mA, V_I = 0 to V_{CC}, V_C = V_{IH} (see Figure 1)	2 V		150				Ω
			4.5 V		50	85		106	
			6 V		30				
$R_{on(p)}$	Peak on resistance	V_I = V_{CC} or GND, V_C = V_{IH}, I_T = −1 mA	2 V		320				Ω
			4.5 V		70	170		215	
			6 V		50				
I_I	Control input current	V_C = 0 or V_{CC}	6 V		±0.1	±100		±1000	nA
I_{soff}	Off-state switch leakage current	V_I = V_{CC} or 0, V_O = V_{CC} or 0, V_C = V_{IL} (see Figure 2)	6 V			±0.1		±5	µA
I_{son}	On-state switch leakage current	V_I = V_{CC} or 0, V_C = V_{IH} (see Figure 3)	6 V			±0.1		±5	µA
I_{CC}	Supply current	V_I = 0 or V_{CC}, I_O = 0	6 V			2		20	µA
C_i	Input capacitance	A or B		5 V		9				pF
		C				3	10		10	
C_f	Feedthrough capacitance	A to B	V_I = 0			0.5				pF
C_o	Output capacitance	A or B		5 V		9				pF

switching characteristics over recommended operating free-air temperature range

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	$T_A = 25°C$			MIN	MAX	UNIT
						MIN	TYP	MAX			
t_{PLH}, t_{PHL}	Propagation delay time	A or B	B or A	C_L = 50 pF (see Figure 4)	2 V		10	60		75	ns
					4.5 V		4	12		15	
					6 V		3	10		13	
t_{PZH}, t_{PZL}	Switch turn-on time	C	A or B	R_L = 1 kΩ, C_L = 50 pF (see Figure 5)	2 V		70	180		225	ns
					4.5 V		21	36		45	
					6 V		18	31		38	
t_{PLZ}, t_{PHZ}	Switch turn-off time	C	A or B	R_L = 1 kΩ, C_L = 50 pF (see Figure 5)	2 V		50	200		250	ns
					4.5 V		25	40		50	
					6 V		22	34		43	
f_I	Control input frequency	C	A or B	C_L = 15 pF, R_L = 1 kΩ, $V_C = V_{CC}$ or GND, $V_O = V_{CC}/2$ (see Figure 6)	2 V		15				MHz
					4.5 V		30				
					6 V		30				
	Control feedthrough noise	C	A or B	C_L = 50 pF, $R_{in} = R_L$ = 600 Ω, $V_C = V_{CC}$ or GND, f_{in} = 1 MHz (see Figure 7)	4.5 V		15				mV (rms)
					6 V		20				

operating characteristics, V_{CC} = 4.5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF,	f = 1 MHz	45	pF
	Minimum through bandwidth, A to B or B to A[†] [20 log (V_O/V_I)] = –3 dB	C_L = 50 pF, $V_C = V_{CC}$,	R_L = 600 Ω, (see Figure 8)	30	MHz
	Crosstalk between any switches[‡]	C_L = 10 pF, f_{in} = 1 MHz	R_L = 50 Ω, (see Figure 9)	45	dB
	Feedthrough, switch off, A to B or B to A[‡]	C_L = 50 pF, f_{in} = 1 MHz	R_L = 600 Ω, (see Figure 10)	42	dB
	Amplitude distortion rate, A to B or B to A	C_L = 50 pF, f_{in} = 1 kHz	R_L = 10 kΩ, (see Figure 11)	0.05%	

[†] Adjust the input amplitude for output = 0 dBm at f = 10 kHz. Input signal must be a sine wave.
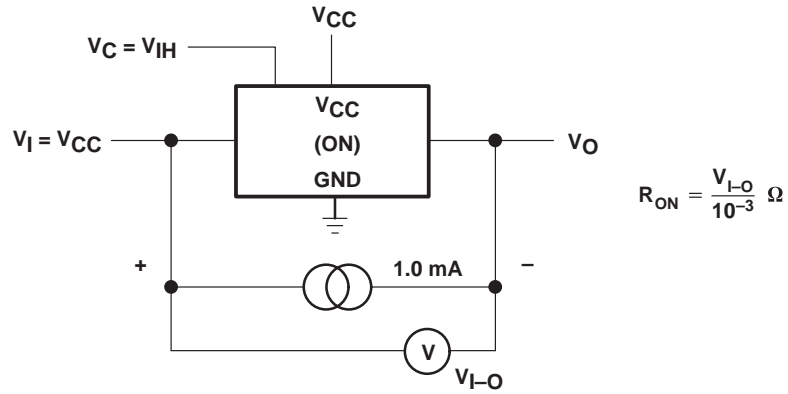[‡] Adjust the input amplitude for output = 0 dBm at f = 1 MHz. Input signal must be a sine wave.

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION

$$R_{ON} = \frac{V_{I-O}}{10^{-3}} \ \Omega$$

Figure 1. On-State Resistance Test Circuit

$V_S = V_A - V_B$
CONDITION 1: $V_A = 0$, $V_B = V_{CC}$
CONDITION 2: $V_A = V_{CC}$, $V_B = 0$
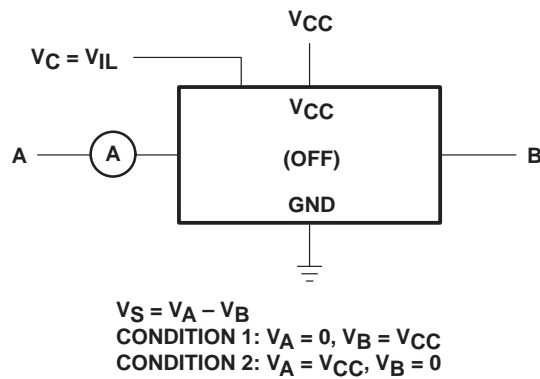
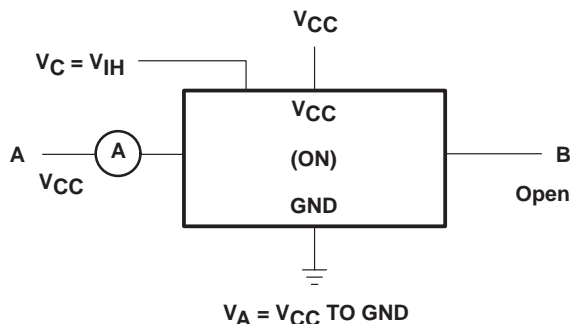**Figure 2. Off-State Switch Leakage Current Test Circuit**

PARAMETER MEASUREMENT INFORMATION
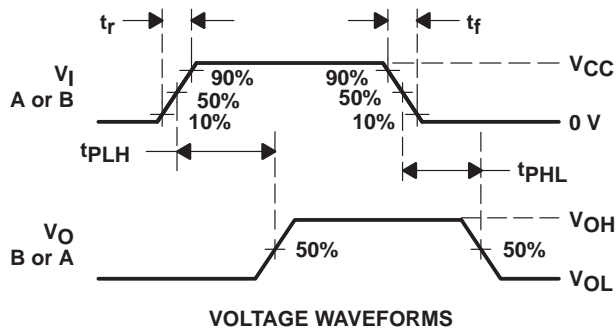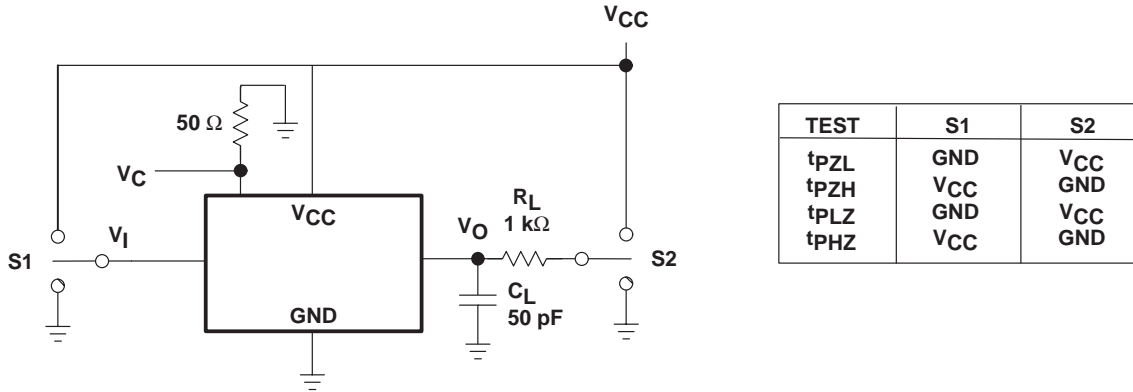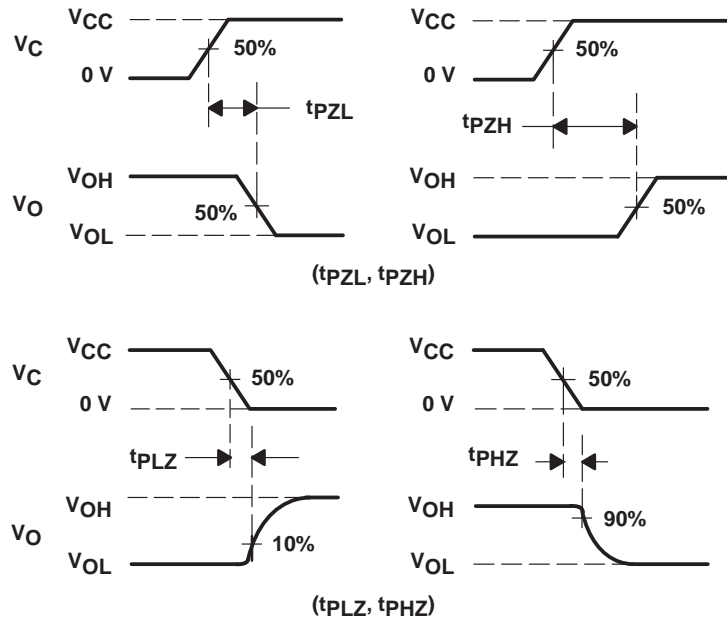

Figure 3. On-State Leakage Current Test Circuit
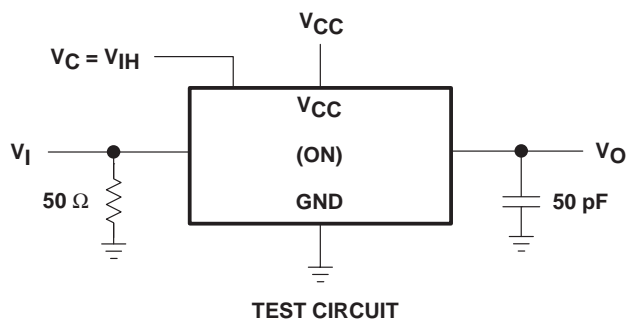
Figure 4. Propagation Delay Time, Signal Input to Signal Output

PARAMETER MEASUREMENT INFORMATION

TEST	S1	S2
t_{PZL}	GND	V_{CC}
t_{PZH}	V_{CC}	GND
t_{PLZ}	GND	V_{CC}
t_{PHZ}	V_{CC}	GND

TEST CIRCUIT

VOLTAGE WAVEFORMS

Figure 5. Switching Time (t_{PZL}, t_{PLZ}, t_{PZH}, t_{PHZ}), Control to Signal Output

PARAMETER MEASUREMENT INFORMATION
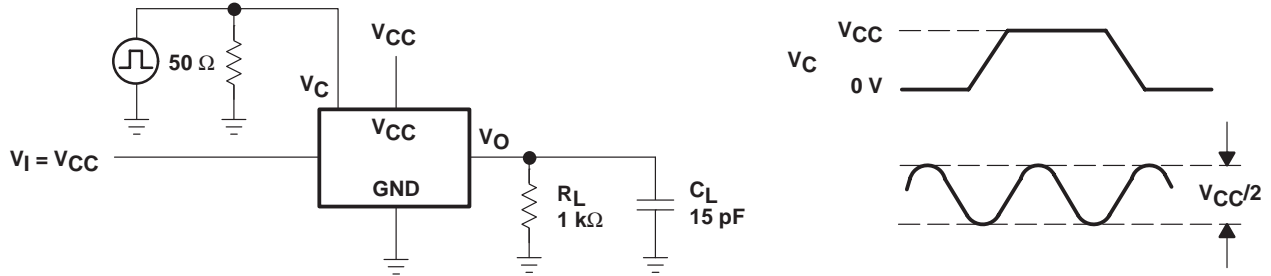
Figure 6. Control Input Frequency
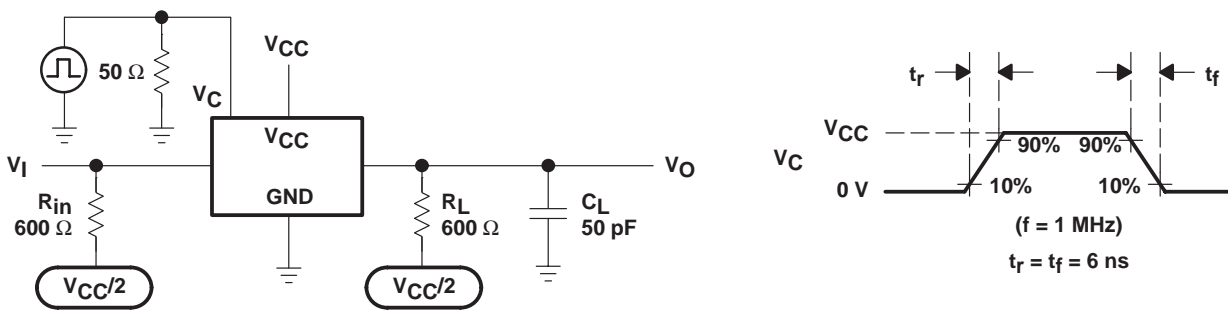
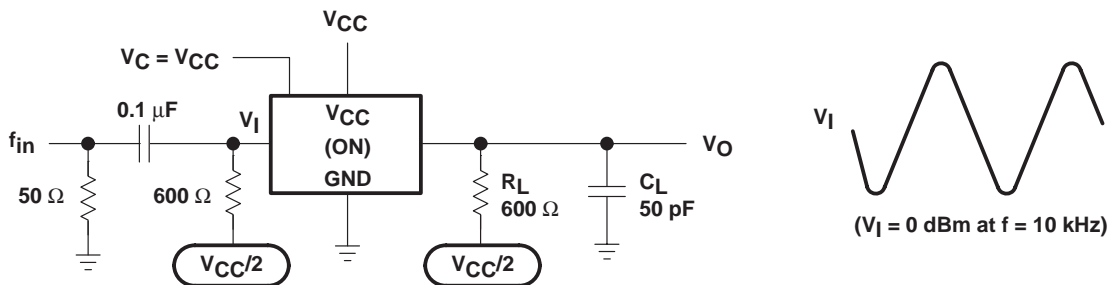**Figure 7. Control Feedthrough Noise**

Figure 8. Minimum Through Bandwidth

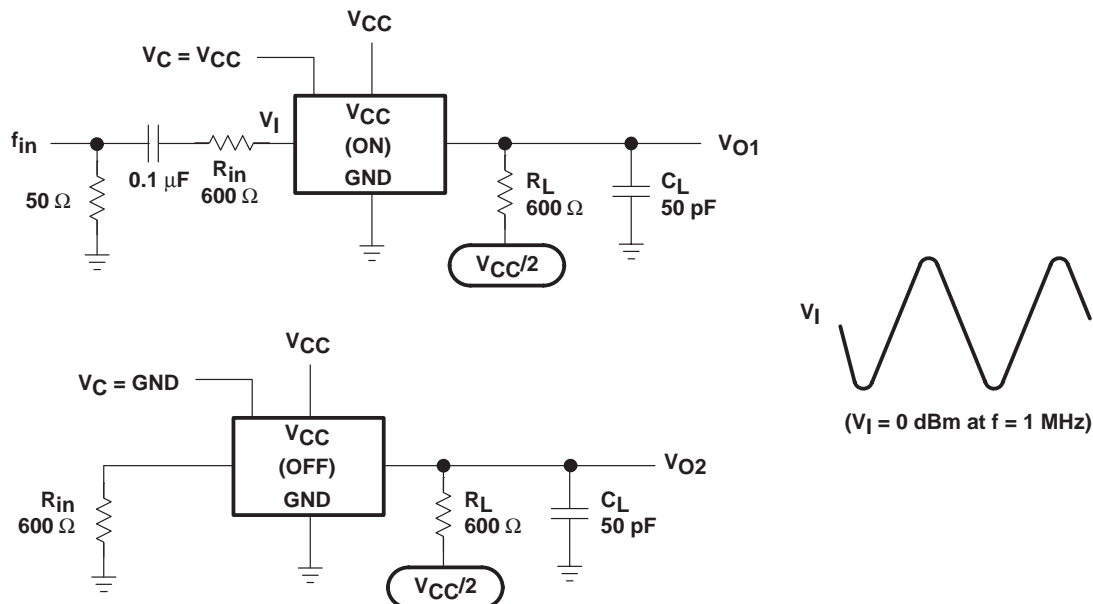## PARAMETER MEASUREMENT INFORMATION
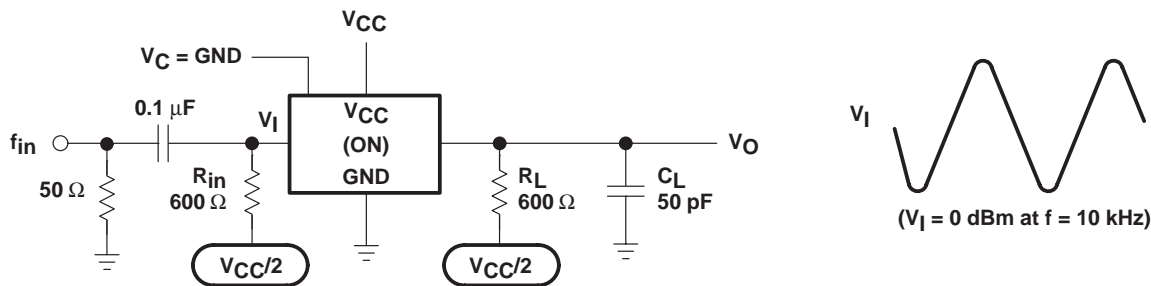

Figure 9. Crosstalk Between Any Two Switches
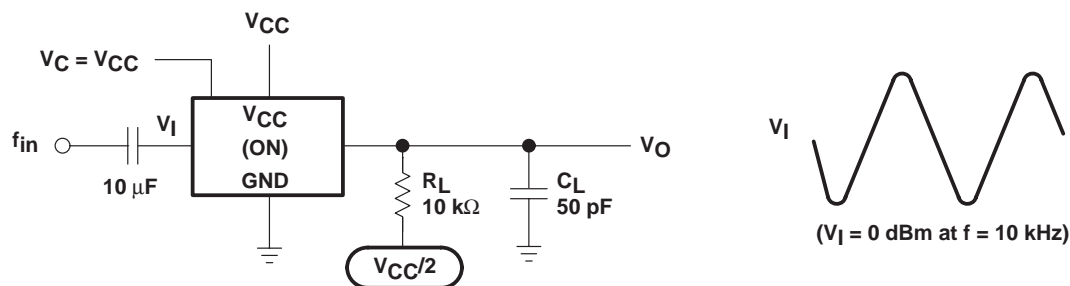

Figure 10. Feedthrough, Switch Off

Figure 11. Amplitude Distortion Rate

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

Copyright © 2000, Texas Instruments Incorporated